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[Title of the Invention] METHOD AND APPARATUS FOR RECORDING AND REPRODUCING DIGITAL SIGNALS
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[Inventor]
[Address] c/o Pasonaru Media Kiki Jigyobu, HITACHI, LTD., 1410, Inada, Hitachinaka-shi, Japan.
[Name] Hitoaki OWASHI
[Inventor]
[Address] c/o Pasonaru Media Kiki Jigyobu, HITACHI, LTD., 1410, Inada, Hitachinaka-shi, Japan.
[Name] Hiroo OKAMOTO
[Inventor]
[Address] c/o Pasonaru Media Kiki Jigyobu, HITACHI, LTD., 1410, Inada, Hitachinaka-shi, Japan.
[Name] Kyoichi HOSOKAWA
[Inventor]
[Address] c/o Pasonaru Media Kiki Jigyobu, HITACHI, LTD., 1410, Inada, Hitachinaka-shi, Japan.
[Name] Takaharu NOGUCHI
[Applicant]
[Applicant's ID Number] 0 0 0 0 0 5 1 0 8
[Postal Code] 101
[Address] 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, Japan.
[Name] HITACHI, LTD.
[Representative Director] Tsutomu KANAI

[Title of Document] Specification

[Title of the Invention] METHOD AND APPARATUS FOR RECORDING AND REPRODUCING DIGITAL SIGNALS

[Scope of Claim for a Patent]

[Claim 1]

A method of recording and reproducing a digital signal for a recording/reproducing apparatus in which:

packeting digital information;

inputting each packet signal with time information indicating a time information of an arrival of the packet; and

recording the packet signal with time information,

said method comprising the steps of:

reproducing the packet signal with time information with the recording/reproducing apparatus; and

changing at least one bit of a time stamp information contained in the reproduced packet signal and outputting digital information with the changed time stamp information.

[Claim 2]

A method according to claim 1, wherein the digital information includes at least one of bit compressed video information, bit compressed audio information, video

program information, and viewing permission information respectively in a packet format.

[Claim 3]

A method according to claim 1, wherein all information bits of the time stamp information contained in the reproduced packet signal are set to 0 level.

[Claim 4]

A method according to claim 1, wherein all information bits of the time stamp information contained in the reproduced packet signal are set to 1 level.

[Claim 5]

A method of recording/reproducing a digital signal in which:

each of a plurality of programs is bit-compressed;

the bit-compressed program is encrypted;

the encrypted programs are time divisionally multiplexed and packeted;

the time divisionally multiplexed programs are modulated with a single carrier;

the modulated signal is transmitted;

the transmitted signal is received;

the received signal is demodulated;

at least one program in a packet format is selected from the demodulated signal;

the selected program in a packet format is decrypted;

a packet signal added with time information indicating an arrival time of each packet included in the decrypted signal in a packet format is inputted; and the packet signal with the time information is recorded,

the method comprising the steps of:

reproducing the recorded packet signal with the time information; and

changing at least one bit of the time stamp information contained in the reproduced packet signal, and outputting digital information with the changed time stamp.

[Claim 6]

In a digital signal recording/reproducing apparatus in which:

digital information is packeted;

inputting a packet signal with time information indicating an arrival of each packet; and

recording the packet signal with the time information,

the apparatus comprising:

means for reproducing the packet signal with the time information; and

means for changing at least one bit of the time stamp information contained in the reproduced packet signal and outputting the results.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Utilization]

The present invention relates to a method and apparatus for recording and reproducing digital signals of movies, programs, and the like transmitted via transmission media such as coaxial cables, telephone lines, and broadcast satellites. More particularly, the invention relates to such a method and apparatus capable of constraining a copy of a recorded digital signal.

[0002]

[Prior Art]

A method of inhibiting a copy of a video signal with a recording/reproducing apparatus is disclosed, for example, in Japanese Patent Laid-open Publication No. 61-288582 (hereinafter called a first Publication). The technique described in this first Publication adds a signal immediately after a synchronization signal of a video signal so that although a television can display this video signal, a video tape recorder (VTR) can record only an image of poor quality.

[0003]

Another Japanese Patent Laid-open Publication No. 4-360068 (hereinafter called a second Publication) discloses techniques of restricting a user to copy data or inhibiting a user to see an image of data, with a data recording/reproducing apparatus.

[0004]

As a method of compressing digital video signals

at a high efficiency, the ITU-T Draft Rec. H. 262 standard called MPEG-2 (Moving Picture Experts Group) is known. MPEG-2 Systems Working Draft is also known which is the transmission standard of video and audio signals compressed by MPEG-2.

[0005]

[Problems that the Invention is to Solve]

The above standards show the techniques of compressing a program and broadcasting it in a digital format. This compression method realizes a large compression rate so that a single transmission channel can broadcast programs four to eight times as many as a conventional analog broadcast. With this technique, services called near video-on-demand are already available in which the same 2-hour movie is repetitively broadcast at an interval of 30 minutes. However, it is impossible to broadcast all programs 24 hours a day for near video-on-demand. Therefore, subscribers have a great need for recording a program and reproducing it at a desired time to watch it.

[0006]

In recording/reproducing a digitally compressed and broadcast program, it can be considered that a received digital signal is expanded and converted into an analog signal to record it with a conventional analog VTR. However, an analog signal recorded in the analog VTR loses a good S/N ratio of digital signals.

[0007]

It is therefore desired to digitally record a digital broadcast signal. However, no technique is disclosed as yet to record a digital signal compressed and broadcast, for example, in conformity with the MPEG standard. Generally, error correction is performed to a sufficient degree during recording/reproducing digital signals so that even if copies are made repetitively, the image quality is not lowered. However, on the other hand, it is difficult to protect the rights of a copyright holder if a copy without image quality degradation is permitted. Techniques for protecting the rights of a copyright holder are disclosed in the above cited first Publication for conventional analog VTRs. The second Publication discloses techniques for restricting a user to copy data or inhibiting a user to see an image of data, with a data recording/reproducing apparatus.

[0008]

However, techniques of recording digital signals compressed in conformity with the MPEG standard and transmitted and of constraining a copy of recorded digital signals are not shown at all.

[0009]

It is an object of the present invention to provide a method and apparatus for efficiently recording a signal compressed and broadcast, for example, in conformity with the MPEG standard, and constraining copies of such

signals.

[0010]

[Means for Solving the Problems]

In order to solve the above problems, the following means are provided. Specifically, in a method of recording/reproducing a digital signal in which each of a plurality of programs is bit-compressed; the bit-compressed program is encrypted; the encrypted programs are time divisionally multiplexed; the time divisionally multiplexed programs are modulated with a single carrier; the modulated signal is transmitted; the transmitted signal is received; the received signal is demodulated; at least one program in a packet format is selected from the demodulated signal; the selected program in a packet format is decrypted; a packet signal added with time information indicating an arrival time of each packet included in the decrypted signal in a packet format is inputted, and the packet signal with the time information is recorded, the method comprising the steps of: reproducing the recorded packet signal with the time information; and changing at least one bit of information bits of the time stamp contained in the reproduced packet signal, and outputting digital information with the changed time stamp.

[0011]

[Operation]

Packet signals with time information are inputted to the recording/reproducing apparatus and

recorded at packed intervals in order to improve a recording efficiency. In reproducing packet signals, packet intervals are changed to the original intervals in accordance with detected time information added to the packet signals and thereafter output from the recording/reproducing apparatus. Since packet signals are recorded after packing the intervals therebetween, it is possible to record them at a signal rate slower than the input signal, allowing efficient recording. By using the time information added to the packet signal, packet signals can be changed to have the original packet intervals, and thereafter they are reproduced. If at least one bit of the added time information is changed for the reproduction and reproduced signals are supplied to, and recorded with, another recording/reproducing apparatus, the original intervals between these signals cannot be restored because the added time information is different from the original time information. Accordingly, these signals cannot be expanded and restored.

[0012]

[Embodiments]

A video distribution service using a satellite according to an embodiment of the invention will be described with reference to Fig. 1. In Fig. 1, a reference numeral 10 designates a software supplier, numeral 20 an operation center, numeral 30 a program distribution center, numeral 31 a transmitter, numeral 35 a current broadcasting

station, numeral 36 a transmitter, numeral 40 an artificial satellite for distributing signals, numeral 50 a subscriber household, numeral 51 a receiver, numeral 52 a receiver decoder, numeral 53 a VTR, numeral 54 a TV receiver, numeral 55 a telephone set, and numeral 56 a receiver.

[0013]

The video distribution service is carried out by an operator managing the operation center 20. The operator signs a contract with the software supplier 10 and causes the required software to be supplied from the software supplier 10 to the program distribution center 30. According to the embodiment shown in Fig. 1, only one supplier 10 is shown. Normally, however, a plurality of software suppliers are engaged in supplying software.

[0014]

The program distribution center 30 transmits a radio wave toward the satellite 40 by means of the transmitter 31 installed in the center 30. The satellite 40 receives the radio wave and retransmits it toward the subscriber 50. The radio wave thus transmitted is received by the receiver 51. According to the embodiment shown in Fig. 1, only one subscriber 50 is shown. Actually, however, a plurality of subscribers exist.

[0015]

The radio wave received by the receiver 51 is applied to the receiver decoder 52, and the software of a predetermined channel is selected by the receiver decoder

52. The software thus selected is recorded in the VTR 53 as required. The signal recorded in the VTR 53 and reproduced at the desired time is returned to the receiver decoder 52, restored into the original video signal, and applied to the TV receiver 54. In the case where the subscriber desires to watch the program without recording, the original video signal is restored without the VTR 53 and applied to the TV receiver 54.

[0016]

The subscriber may request a desired software from the operation center 20 by way of the telephone 55. Also, the operation center 20 can survey the receiving and viewing conditions of the subscriber 50 through the telephone channel from the receiver decoder 52 and charge the subscriber 50 in accordance with the viewing conditions.

[0017]

Further, the radio wave transmitted from the current broadcast station 35 by the transmitter 36 is received by the receiver 56 and the received signal is input and recorded in the VTR 53. The signal reproduced in the VTR 53 may be applied to the TV receiver 54 to view the program. In the case where the VTR 53 is not required to record the program, the signal from the receiver 56 is of course applied to the TV receiver 54 and the program can be viewed directly.

[0018]

Fig. 2 is a block diagram showing the details of the program distribution center 30. In Fig. 2, reference numeral 100 represents input means for inputting software sent from the software supplier 10, numeral 101 represents input means for inputting a control signal of a program or the like sent from an operation center 20, numeral 110 represents reception processing means for preforming a reception process, if necessary, of software input from the input means 100, numerals 111, 120, and 131 represent storage media such as a digital VTR, numeral 112 represents a change-over circuit, 121 and 130 represent bit compressors, numeral 140 represents a transmission processing device, and numeral 150 represents a program controller.

[0019]

Programs are supplied from the software supplier 10 to the program distribution center 30 via communication channels such as optical fibers, coaxial cables, or broadcast satellites. Programs may be supplied by storage media such as VTR cassettes and optical disks. If software is supplied via communication channels, it is input via the input means 100 to the reception processing device 110. The reception processing device 110 performs modulation, error correction, bit expansion, or the like of the input signal, if necessary. An output signal from the reception processing device 110 is input to the change-over circuit 112 and storage media 120, the latter storing the input

software therein. If software in the form of storage media such as VTR cassettes and optical disks is supplied from the software supplier 10 to the program distribution center 30, it is reproduced by the storage media 111 matching the type of the supplied software. A program reproduced by the storage media 111 is input to the change-over circuit 112.

[0020]

The change-over circuit 112 selects a proper input signal and outputs it to the bit compressor 130. The bit compressor 130 performs digital signal compression, for example, by MPEG, to reduce the data amount necessary for transmission. If digitally compressed data is supplied from the soft supplier 10, the bit compressor 130 may be omitted. An output signal of the bit compressor 131 is input to the storage media 131. As the storage media 131, media capable of recording/reproducing data such as digital VTRs, optical disks, and magnetic disks may be used.

[0021]

A control signal for a program or the like sent from the operation center 20 via the input means 101 is input to the program controller 150. This program transmission control signal of the program controller 150 is input to the storage media 120 and 131 and transmission processing device 140. In accordance with this control signal, necessary software is output from the storage media 120 and 131. Software output from the storage media 120 is input to the bit compressor 121 which like the bit

compressor 130 performs digital compression, for example, by MPEG-2, to reduce the data amount necessary for transmission. An output signal from the bit compressor 121 is input to the transmission processing device 140. A signal output from the bit compressor 131 is also input to the transmission processing device 140.

[0022]

If software supplied from the software supplier 10 is intended to be immediately transmitted, the software once stored in the storage media 120 is not output, but the input signal to the bit compressor 121 is directly output, while recording it in the storage media 120 if necessary.

[0023]

If data of software supplied from the software supplier 10 is already bit-compressed, it is not necessary to supply it to the bit compressor 121. In the embodiment shown in Fig. 2, only two inputs to the transmission processing device 140 are shown. However, a larger number of inputs may be supplied to the transmission processing device 140. Furthermore, only one transmission channel is shown, a plurality of combinations constituted by the storage media 120 and 131, bit compressor 121, and transmission processing device 140 may be provided to transmit signals via a plurality of transmission channels.

[0024]

The transmission processing device 140, in accordance with the necessity, encrypts each program,

packets it, time-division multiplexes a plurality of programs, adds transmission error correction codes, and modulates each packet signal so as to transmit it over a predetermined transmission channel in accordance with the control signal from the program controller 150. An output signal from the transmission processing device 140 is input to the transmitter 31 which transmits a signal toward the satellite 40 shown in Fig. 1.

[0025]

Fig. 3 is a block diagram showing the program distribution center 30 according to another embodiment in detail. Elements shown in Fig. 3 are partially used in common with Fig. 2, and like elements to those shown in Fig. 2 are represented by using the identical reference numerals and the detailed description thereof is omitted. In Fig. 3, reference numeral 115 represents a supply unit for a storage medium, numerals 160 to 163 storage media, numerals 170 to 173 bit compressors, numeral 180 a transmission processing device, numeral 190 a program controller, and numeral 191 a program guide generator.

[0026]

The embodiment shown in Fig. 3 represents the case in which software is sent from the software supplier 10 in a storage medium. In this case, the terminal 100 acts only as a reception window for receiving the storage medium by the program distribution center 30. The storage medium thus received is stored in a storage medium supply

unit 115 on the one hand and is supplied to the storage media 160 to 163 under the control of the program controller 190. The signals reproduced at the storage media 160 to 163 are applied respectively to the bit compressors 170 to 173, where they are bit-compressed according to the MPEG-2 standard or the like. The output signal of the compressors 170 to 173 is applied to the transmission processing device 180.

[0027]

Also, a control signal for the program issued or the like is applied from the operation center 20 through the input means 101 to the program controller 190. The program issue control signal from the program controller 190 is applied to the storage medium supply unit 115, the storage media 160 to 163 and the transmission processing device 180. In accordance with this control signal, as described above, the storage medium in the storage medium supply unit 115 is supplied to the storage media 160 to 163 thereby to control the reproduction, termination, etc. of the software of the storage media 160 to 163.

[0028]

Further, the guide information for the program distributed to the subscriber 50 from the program distribution center 30 is generated in the program guide generator 191 in accordance with the information from the program controller 190, and applied to the transmission processing device 180. The transmission processing device

180 processes signals for transmission in accordance with, for example, the MPEG transmission standard described above. The signal thus processed for transmission is applied to the transmitter 31 and transmitted toward the satellite 40 from the transmitter 31.

[0029]

Fig. 4 is a block diagram showing an example of the signal processing operation in the transmission processing device 180. In Fig. 4, numerals 170a to 173a, 190a, 191a designate input terminals, numerals 170b to 173b, 31a output terminals, numerals 181 to 184 encryptors, numeral 185 a time-division multiplexer, numeral 186 an error correction code adder, and numeral 187 a modulator.

[0030]

In Fig. 4, the signals from the bit compressors 170 to 173 are applied through the input terminals 170a to 173a to the encryptors 181 to 184, respectively. The encryptors 181 to 184 encrypt the supplied programs as required. This encryption may be effected only on the video signal or the audio signal, or on both the video signal and the audio signal. The signal thus encrypted is applied to a time-division multiplexer 185. The terminal 190a is an input terminal for the signals from the program controller 190. The viewing right control signal for each program is applied through the terminal 190a to the time-division multiplexer 185. This signal includes a signal indicating whether a particular subscriber has the viewing

right for the signal broadcast. Further, the time-division multiplexer 185 is supplied with program guide information from a program guide generator 191 through the input terminal 191a. Each signal is packeted in a predetermined format and compressed and multiplexed temporally. According to this embodiment, the viewing right control signal and the program guide information are shown without an encryptor. These signals, however, may also be encrypted.

[0031]

The rate control information for each program is applied through the terminal 190a. This is the information for bit-compressing the program input from the bit compressor 170 in the range of 4 to 8 Mbps, and the program input from the bit compressor 171 in the range of 2 to 6 Mbps, for example. According to this information, the time-division multiplexer 185 controls the bit rate of the bit compressors 170 to 173. The time-division multiplexer 185 applies a control signal to the bit compressors 170 to 173 through the output terminals 170b to 173b. As a result, the bit rate of each program is controlled in such a way that the signal rate after time-division multiplexing is less than a predetermined value.

[0032]

The output signal of the time-division multiplexer 185 is applied to the error correction code adder 186. In the case under consideration, an error

correction code is added for correcting the transmission error caused by the noise in a satellite channel, a CATV channel, and the like. The output signal of the error correction coder is applied to the modulator 187, and in the case of the embodiment shown in Fig. 3, the programs of four channels are modulated on a single carrier thereby constituting a single transmission channel. The signal modulated on the single carrier is sent toward the transmitter 31 through the terminal 31a.

[0033]

An output signal of the transmission processing device 180 is input to the transmitter 31. The operation to follow is the same as the embodiment shown in Fig. 2. Although the embodiment shown in Fig. 3 has four storage media so that the transmission processing device 180 can be supplied with four programs, more programs can be time-division multiplexed by use of more storage media.

[0034]

According to the embodiment shown in Fig. 3, signals for a single transmission channel are processed. Instead, signals for a plurality of transmission channels can be sent by providing a plurality of combinations of the storage media 160 to 163, the bit compressors 170 to 173 and the transmission processing device 180.

[0035]

The transmission channel is defined as a signal modulated on a single carrier by time-division multiplexing

a plurality of programs as described above. Each of a plurality of programs is referred to simply as a channel.

[0036]

Fig. 5 shows a specific example of the configuration of a receiver decoder at the subscriber household 50. In Fig. 5, numeral 200 designates an input terminal for a signal from the receiver 51, numeral 201 an input-output terminal for a signal for requesting a software from the operation center or a signal for exchanging the signal for determining the receiving conditions of a fee-charging broadcast, numeral 202 an output terminal for a signal restored, numeral 203 an input-output terminal for a signal exchanged with the VTR, numeral 205 an input terminal for a signal from the receiver 56 shown in Fig. 1, numeral 210 a tuner, numeral 220 an error correction circuit, 230 a program dividing circuit, numeral 240 a change-over circuit, numeral 250 a decryption circuit, numeral 260 a decoding circuit for bit expansion, numeral 270 a signal output processing circuit, numeral 280 a control circuit, and numeral 290 an interface circuit.

[0037]

The receiver 51 that has received a signal from the satellite 40 applies the received signal to the tuner 210 through the terminal 200. The tuner 210 selects from among the received signals the signal of a desired transmission channel in accordance with the control signal from

the control circuit 280, and demodulates the signal modulated by the modulator 187 of the transmission processing device 140, 180 and applies the demodulated signal to the error correction circuit 220. The error correction circuit 220 corrects any error occurred mainly in the channel in accordance with the error correction code added by the error correction code adder 186 of the transmission processing device 140, 180. The signal the error of which has been corrected is applied to the program dividing circuit 230 of the transmission processing device 140, 180. The program dividing circuit 230 selects and outputs a desired program in accordance with the control signal from the control circuit 280 from a plurality of programs time-division multiplexed by the time-division multiplexer 185 of the transmission processing device 140, 180 on a single transmission channel.

[0038]

The output signal of the program dividing circuit 230 is applied to the change-over circuit 240 and the interface circuit 290, and further through the terminal 203 to the VTR 53. The VTR 53 records the digital bit stream applied thereto, and at playback, applies a signal to the interface circuit 290 through the terminal 203 in the same format as the input bit stream. The output signal of the interface circuit 290 is applied to the change-over circuit 240. The change-over circuit 240 selects and outputs a signal from the program dividing circuit 230 when restoring

the received signal and selects and outputs a signal from the interface circuit 290 when selecting and outputting a reproduced output signal of the VTR 53, in accordance with the control signal from the control circuit 280.

[0039]

The output signal of the change-over circuit 240 is applied to the decryption circuit 250. The decryption circuit 250 decrypts the signal encrypted by the encryptors 181 to 184 of the transmission processing device 140, 180. The signal decoded from the code produced by the decryption circuit 250 is applied to the decoding circuit 260, where the bits compressed at the bit compressors 160 to 163 shown in Fig. 3 or at the soft supplier 10 shown in Fig. 1 are decoded and decompressed.

[0040]

The bit-decompressed signal from the decoding circuit 260 is applied to the output processing circuit 270 as a component signal containing a luminance signal and two color difference signals. The two color difference signals applied to the output processing circuit 270 are subjected to quadrature modulation and thus converted into a carrier chrominance signal, so that the output processing circuit 270 produces the resulting carrier chrominance signal and the luminance signal. The output signal is applied through the terminal 202 to the TV receiver 54. Just in case the TV receivers 54 has only a composite input terminal, the output processing circuit 270 may produce a composite

signal by adding the luminance signal and the carrier chrominance signal. Further, both a signal containing the luminance signal and the carrier chrominance signal and a composite signal may be produced.

[0041]

Also, the signal applied from the receiver 56 through the input terminal 205 is recorded in the VTR 53 if necessary, and a reproduced signal or, if not recorded, an input signal or a signal equivalent to the input signal, is applied to a TV image pick-up device 54. In the embodiment shown in Fig. 5, the signal not yet decrypted is recorded in the VTR 53, and therefore the signal is not necessarily decrypted at the time of recording in the VTR 53. The subscriber thus can record free of charge and can be charged each time of playback.

[0042]

Fig. 6 shows another specific example of the receiver decoder shown in Fig. 1 according to an embodiment. The component parts included in Fig. 6, which are partially shared by the embodiment of Fig. 5, are designated by the same reference numerals as the corresponding parts respectively and will not be described in detail.

[0043]

According to the embodiment shown in Fig. 6, the change-over circuit 240 is located behind the decryption circuit 250 as compared with the embodiment shown in Fig.4.

Specifically, the output signal of the decryption circuit 250 is applied to the VTR 53 and the change-over circuit 240, and the output signal of the VTR 53 to the change-over circuit 240. The output signal of the change-over circuit 240 is applied to the decoding circuit 260.

[0044]

The embodiment shown in Fig. 6 concerns the case of recording a signal decrypted at the decryption circuit 250. In this case, the decrypted signal is recorded in the VTR 53. Therefore, the subscriber is charged for decryption at recording, and can playback without being charged.

[0045]

Although the decryption circuit 250 is arranged behind the program dividing circuit 230 in the embodiment shown in Fig. 6, the program dividing operation may be performed after decryption.

[0046]

Fig. 7 is a block diagram showing a VTR 53 according to an embodiment. In Fig. 7, numeral 300 designates an input-output terminal for a signal from the receiver decoder 52 shown in Fig. 1, numeral 302 an input terminal for a signal from the receiver 56 shown in Fig. 1, numeral 303 an output terminal thereof, numeral 305 an interface circuit, numeral 311 a parity adder circuit, numeral 312 a modulation circuit, numeral 320 a tape transport system, numeral 330 a demodulation circuit,

numeral 331 an error correction circuit, numeral 340 an analog video signal recording circuit, numeral 350 an analog video signal reproduction circuit, numeral 360 an analog audio signal recording circuit, and numeral 370 an analog audio signal reproduction circuit.

[0047]

The signal applied through the input terminal 300 is applied to the parity adder circuit 311 through the interface circuit 305. The parity adder circuit 311 is for adding a parity code for correcting any error which may occur in the tape transport system 320. The output signal from the parity adder circuit 311 is applied to the modulation circuit 312. The modulation circuit 312 modulates the digital signal into a form suitable for the tape transport system 320. Such schemes as NRZ, NRZI, 8-10 conversion, MFM, M2, etc. are known for modulation. The modulated signal is applied to the tape transport system 320 and recorded in the magnetic tape 1.

[0048]

At playback, the reproduced signal is applied to the demodulation circuit 330 where it is modulated in correspondence with the modulation circuit 312. The output signal of the demodulation circuit 330 is applied to the error correction circuit 331, where any error which may have occurred in the tape transport system 320 is corrected on the basis of the parity code added at the parity adder circuit 311. The output signal of the error correction

circuit 331 is applied to the interface circuit 305, and after being converted into a signal in the same form as the signal input from the input terminal 300, is output from the terminal 300. The signal output from the terminal 300 is applied to the receiver decoder 52 shown in Fig. 1.

[0049]

As seen from the embodiment of Fig. 7, the VTR 53 requires therein none of the bit compressors 121 to 130 shown in Fig. 2, and therefore a digital signal VTR small in circuit size can be realized. Also, no bit compressor is required in each VTR, but only at the soft supplier 10 or program distribution center 30. Therefore, although the circuit size and cost increase, a high-performance bit compressor can be used, and the resulting higher relative bit compression ratio reduces the data rate of the digital signal transmitted. Consequently, the VTR 53 used by the subscriber can be improved in quality, reduced in cost and can record for a longer time.

[0050]

An analog signal is applied through the terminal 302 from the receiver 56 to the analog video signal recording circuit 340 and the analog audio signal recording circuit 360, where the signal is processed according to the VHS standard, beta standard or the 8-mm VTR standard, for example. The signal thus processed is applied to the tape transport system 320. The tape transport system 320 records the signal in accordance with respective formats

as in the conventional VTR.

[0051]

At playback, the signal reproduced at the tape transport system 320 is applied to the analog video signal reproduction circuit 350 and the analog audio signal reproduction circuit 370 which process the reproduced signal in a manner corresponding to the analog video signal recording circuit 340 and the analog audio signal recording circuit 360, respectively. The reproduced signal is applied appropriately to the TV receiver 54 shown in Fig. 1 through the output terminal 303. As a result, the digital broadcast and the conventional analog broadcast can be recorded using the same tape transport system.

[0052]

Fig. 8 is a model diagram showing an example signal (or an output signal from the output terminal 31a shown in Fig. 4) output from the transmitter 31, in the embodiments shown in Figs. 2 and 3. The embodiment of Fig. 8 shows the case in which four programs are transmitted through a single transmission channel according to the embodiment shown in Fig. 3. Also, the embodiment concerns the case in which there are a number n of transmission channels (1) to (n). In Fig. 8, V1, V2, V3 and V4 designate video signals of four programs, A1, A2, A3, A4 audio signals for four programs, PG a signal representing program guide information, and VECM, AECM a control signal representing the viewing rights. Each of these signals is

a signal constituting a packet.

[0053]

In the embodiment shown in Fig. 3, the four programs generally have different transmission rates. From the instantaneous point of view, the data amount is increased or decreased. In order to efficiently control this variation, each information is packeted and time-division multiplexed as shown in Fig. 8. Details of the signal in the packet are described in the transmission standards referred to above. Though not shown in detail in the model diagram of Fig. 8, the signal in each packet is encrypted by the encryptors 181 to 184 as required as explained with reference to Fig. 4. Also, the error correction code adder 186 adds an error correction code and the time-division multiplexer 185 header information such as a synchronization signal.

[0054]

In the embodiments shown in Figs. 5 and 6, signals designated by (1) to (n) in Fig. 8 are supplied through the terminal 200, and a signal for one of the transmission channels is selected at the tuner 210. In the case under consideration, the signal of Fig. 8(1) is assumed to have been selected. The selected signal shown in Fig. 8(1) has an error thereof corrected at the error correction circuit 220 and is applied to the program dividing circuit 230. The program indicated by the suffix 1 is assumed to have been selected from the time-division

multiplexed four programs at the program dividing circuit 230. In such a case, the program guide information PG, the viewing right control signals VECM, AECM are also separated and output at the same time as the video signal V1 and the audio signal A1. Fig. 9(2) shows the signal representing a divided program. Fig. 9(1) is identical to Fig. 8(1).

[0055]

With reference to the embodiments shown in Figs. 5 and 6, explanation will first be made about the case in which not the reproduced signal from the VTR 53 but the signal from the tuner 210 is selected directly by the change-over circuit 240. The signal divided into a program shown in Fig. 9(2) is decrypted by the decryption circuit 250. This decryption is performed according to the viewing right control signals VECM, AECM shown in Fig. 9(2). More specifically, in the case where a subscriber household has the right to view the program selected just now, the code is decrypted, while when the subscriber household has no right to view the program, the code is not decrypted. Instead, the absence of the viewing right is indicated or information indicating a method for acquiring the viewing right is output from the terminal 202. The output of this information is what is called an OSD. This information is added to the video signal and output from the output processing circuit 270.

[0056]

The signal decrypted is applied to the decoding

circuit 260. The decoding circuit 260 corresponds to the bit compressors 121 and 130 shown in Fig. 2 and the bit compressors 170 to 173 shown in Fig. 3, and decodes a signal input according to the MPEG-2 standard, for example. In the case where a signal compressed according to the MPEG standard is decoded, it is necessary to synchronize the transmitted signal with the data to be decoded. In the case where the transmitted signal fails to be synchronized with the data to be decoded and the decoding rate is higher than the transmission rate, for example, the data runs short making the decoding impossible. In order to prevent such an inconvenience, a clock reference called SCR or PCR is added to the packet according to the MPEG standard. At decoding, the decoding clock signal is restored according to this clock reference. This is described, for example, in MPEG-2 "Latest MPEG Text with Illustrated Points", first edition, published on August 1, 1984 by K.K. Ascii. As a result, the arrival time of each packet cannot be changed.

[0057]

For the selected signal of Fig. 9(2) to be recorded in the VTR 53, therefore, it is necessary to conceive a method for making reproduction while maintaining time intervals of input packets.

[0058]

A signal corresponding to Fig. 9(2) is applied as an input signal to the interface circuit 290. As an example, the bit rate of the signal output from the

transmitter 31 shown in Figs. 2 and 3 is assumed to be 40 Mb/s. Among these bits, assume that the information in the amount 7/6 is assigned for error correction and that the header information of 17 bytes is added for 130 bytes of packets compressed by the bit compressor. Under the condition where an error is corrected by the error correction circuit 220 shown in Figs. 5 and 6 and the header information required for transmission is removed, the bit rate is about 30 Mb/s as expressed by the following Equation (1):

[0059]

$$40 \times (6/7) \times (139/147) = 30.3 \quad \ldots \text{(Equ. 1)}$$

As shown in Fig. 9(2), packets exist successively at some parts and with intervals of several packets at other parts. For the VTR 53 to record while maintaining these time intervals of signals, a recording at higher rate than shown in Equation 1 is required. As shown in Fig. 9(2), packets are not sent for some time intervals. As far as packets can be packed for recording and restored to the original time intervals at the time of reproduction, therefore, the recording rate can be reduced as compared with the value shown in Equation 1. Fig. 9(3) shows signals applied to the VTR 53 from the interface circuit 290 in Figs. 5 and 6 for recording the packets in packed state at the time of recording and restoring the packet intervals to the original time intervals at the time of reproduction.

[0060]

Fig. 9(3) shows signals applied to the interface circuit 290 from the program dividing circuit 230 in the embodiment shown in Fig. 5 and from the decryption circuit 250 in the embodiment shown in Fig. 6. The interface circuit 290 adds information (time stamp) indicating the time of packet arrival as header information to the input signal. Another information than the time stamp may be further added as header information. Also, it is necessary to increase the packet transmission rate in order to add the header information such as a time stamp to the input signal to the interface circuit 290 shown in Fig. 9(2). Fig. 9(3) shows a model of such a case. More specifically, a packet is transmitted for a shorter transmission time in Fig. 9(3) than in Fig. 9(2).

[0061]

Fig. 10 shows a circuit for adding a time stamp according to an embodiment. Numeral 400 designates an input terminal for a clock signal to count the time stamp, numeral 401 an input terminal for a packet signal shown in Fig. 9(2), numeral 402 an output terminal for a signal to which a time stamp is added, numeral 410 a counting circuit, numeral 411 a latch circuit, numeral 420 a memory, numeral 430 a packet head detection circuit, numeral 431 a memory control circuit, numeral 440 a multiplexing circuit, and numeral 450 a delay circuit.

[0062]

The packet signal shown in Fig. 9(2) is applied through the terminal 401 to the memory 420 and the packet head detection circuit 430. The packet head detection circuit 430 detects the head of the packet of the signal input, and the resulting detection signal is applied to the latch circuit 411, the control circuit 431 and the delay circuit 450. The clock signal supplied from the terminal 400, on the other hand, is applied to the counting circuit 410 thereby to count the clock signals continuously. The output signal from the counting circuit is applied to the latch circuit 411. The latch circuit 411 latches the count input by the packet head signal from the packet head detection circuit 430. The count thus latched is applied to the multiplexing circuit 440. This count provides time stamp information for a packet.

[0063]

A control signal for the memory 40 is generated on the basis of the packet head detection signal applied to the control circuit 431. The clock signal applied from the terminal 404 is used as a write clock for the memory 420. This is by reason of the fact that the clock signal coincides with the packet signal frequency applied from the terminal 401. The clock signal applied from the terminal 403 is used as a read clock for the memory 420. A frequency higher than that of the write clock applied from the terminal 404 is selected as a frequency of this clock

signal. In the case where the write clock frequency is 30.3 MHz according to Equation 1, for example, the read clock frequency is set to 49.152 MHz. This read clock constitutes a bus clock frequency of the signal sent to the VTR 53 from the terminal 203 shown in Figs. 5 and 6. In the process, the clock signal for the counting circuit 410 applied from the terminal 400, i.e., the clock signal frequency for the time stamp is the same as the clock signal frequency applied from the terminal 403, for example. In this case, the same signal can be used for the bus clock signal applied from the terminal 403 as the clock signal for the time stamp. This is, however, not to limit the time stamp clock frequency to the same frequency as the bus clock frequency.

[0064]

A predetermined length of time after a packet is applied to the memory 420, the packet is read from the memory. The frequency of the read clock signal is set higher than the write clock signal frequency. Therefore, the transmission time of the output packet can be reduced as compared with the transmission time of the input packet signal as shown in Figs. 9(2) and 9(3). As a result, even where a succession of packets are transmitted, as shown in Fig. 9(3), a period of time is available for adding the header information including the time stamp. The output signal of the memory 420 is applied to the multiplexing circuit 440.

[0065]

The delay circuit 450 delays the packet head detection signal and outputs a gate signal indicating the position of addition of the time stamp signal in accordance with the packet signal output from the memory 420. The particular gate signal is applied to the multiplexing circuit 440, where the time stamp from the latch circuit 411 is added and the signal shown in Fig. 9(3) is output from the terminal 402 in accordance with the gate signal.

[0066]

The signal shown in Fig. 9(3) is applied through the terminal 203 shown in Figs. 5 and 6 to the VTR 53. Fig. 11(1) shows signals corresponding to Fig. 9(3), and characters P1, P2,.... designate input packet signals. In the VTR 53, as shown in Fig. 7, the packet signals P4, P5,.. shown in Fig. 11(1) are applied to the parity adder circuit 311 through the terminal 300 and the interface circuit 305. The parity adder circuit 311 includes a memory (not shown) of a capacity for storing at least as many signals as to be recorded in a single track, which memory stores the packet signals P4, P5,... The parity adder circuit 311 outputs packet signals in packed state as shown in Fig. 11(2). There are gaps formed between the packets of the input signal shown in Fig. 11(1) as explained with reference to Fig. 9. Since the packet signals are output with the gaps thereof closed, as shown in Fig. 11(2), however, the rate of the output signal is

lower than that of the input packet signals. The recording rate for the tape transport system 320 can thus be reduced. In Fig. 11, the output signal (2) are shown delayed behind the input signal (1) by a track of period for the sake of simplicity. However, the delay is not limited to a track of period but may be as required for the signal processing.

[0067]

At the time of reproduction, the signal reproduced and output from the tape transport system 320 is applied through the demodulation circuit 330 to the error correction circuit 331. The signal applied to the error correction circuit 331 is, as in the case of Fig. 11(2), composed of packet signals P1, P2,.... in packed state. Fig. 11(3) shows a reproduced input signal for the error correction circuit. The error correction circuit 331 also has a memory (not shown) of a capacity corresponding to the signal for one track period. The input signal shown in Fig. 11(3) is applied to the memory in the error correction circuit 331. Fig. 12 is a block diagram showing an embodiment of a temporal adjusting circuit for restoring the intervals of the reproduced packet signals P1, P2,... to the original length. Fig. 11(4) shows the reproduced packet signals P1, P2,.... whose intervals are restored to the original length.

[0068]

In Fig. 12, numeral 510 designates a memory in the error correction circuit 331, numeral 500 an input

terminal for the memory 510, numeral 520 a memory, numeral 501 a read clock input terminal for the memory 520, numeral 502 a write clock input terminal for the memory 520, numeral 503 an output terminal for the signal temporally adjusted, numeral 551 a counting circuit, numeral 504 an input terminal for the clock signal for the counting circuit 551, numeral 530 a time stamp gate circuit, numeral 540 a control circuit, numeral 550 a time stamp read circuit, numeral 552 a coincidence detection circuit, numeral 560 a circuit block built in the error correction circuit 331, and numeral 570 a circuit block built in the interface circuit 305.

[0069]

The reproduced signal shown in Fig. 11(3) applied from the terminal 500 shown in Fig. 12 is applied to the memory 510. The signal output for each of the packets represented by the packet signals P1, P2,.... from the memory 510 is applied to the memory 520 and the time stamp read circuit 550. The read operation of the memory 510 and the write and read operation of the memory 520 are controlled by the control signal from the control circuit 540. The time stamp read circuit 550 is also supplied with the control signal from the control circuit 540 and outputs a signal indicating the position of the time stamp signal with respect to the signal from the memory 510, thereby reading the time stamp signal at the correct position. The time stamp signal thus read is applied to the coincidence

detection circuit 552.

[0070]

A clock signal of the same frequency as that input from the terminal 400 shown in Fig. 10 is applied from the terminal 504 to the counting circuit 551. The counting circuit 551 counts the clock signal thus input and outputs the count to the coincidence detection circuit 552. The coincidence detection circuit 552 outputs a coincidence signal when the two input signals coincide with each other, which coincidence signal is applied to the control circuit 540.

[0071]

The control circuit 540 causes a packet signal to be read from the memory 520 in accordance with the coincidence signal. Fig. 11(4) shows a signal thus read out. The read operation is performed in accordance with the read clock signal applied from the read terminal 501. At the same time, a new packet is applied from the memory 510, and is written in the memory 520 on the basis of the write clock applied from the terminal 502. The clock signal frequency applied from the terminal 501 is determined in such a manner as to correspond to the signal rate between the terminal 203 and the VTR 53 shown in Figs. 5 and 6.

[0072]

The packet signals P1, P2,....temporally adjusted and output from the memory 520 are applied to a time stamp

gate circuit 530. The time stamp gate circuit 530 gates the time stamp signal as required, so that all the time stamp signals are fixed to 0 or 1 level, for example. As shown in Fig. 11(5), the signal rearranged to the same time intervals as the signal shown in Fig. 11(1) from the terminal 300 shown in Fig. 7 is output from the terminal 503.

[0073]

As a result of the above-mentioned operation, signals of the same packet intervals as the one shown in Fig. 9(3) are applied from the terminal 203 shown in Figs. 5 and 6 to the interface circuit 290. The interface circuit 290 deletes the header information as required and applies the resulting signal to the switch circuit 240. Hence, the same signal as the one from the tuner 210 applied from the other input terminal of the switch 240 is restored.

[0074]

A VTR for recording digital signals has a feature that the image quality is not deteriorated after repetitive dubbing due to the sufficient error correction effected as shown in Fig. 7. Nevertheless, repeated dubbing without a deterioration of image quality may fail to protect the rights of copyright holders sufficiently. In order to avoid this inconvenience, there is provided a technique for preventing dubbing according to the invention.

[0075]

As shown in Fig. 12, the temporally adjusted packet signals P1, P2,.... output from the memory 520 are applied to the time stamp gate circuit 530. The time stamp gate circuit 530 sets all the signals for the period corresponding to the time stamp shown in Fig. 9(3) to, say, 0 level or 1 level, as described above. As a result, the information indicating the time intervals of the packets disappears from the packet signals P1, P2,.... output from the interface circuit 305 shown in Fig. 7. When the output signal from the terminal 300 is applied to and recorded in the VTR shown in Fig.7, therefore, the signal shown in Fig. 11(3) is reproduced. Since the signal indicating the time stamp position included in each packet which may be read contains no information indicating the time intervals, the original time intervals cannot be restored. In the case where all the signals at the position corresponding to the time stamp are at 0 or 1 level, the circuit shown in Fig. 12, after reading a packet, reads the next packet after the lapse of a time corresponding to the number of bits of the time stamp. Generally, the number of bits of a time stamp is set longer than one track period. The signal of the next track, therefore, is written in the memory 510 before all the packet signals are read from the memory 510. As a result, it is no longer possible to output signals corresponding to input signals. Thus the dubbing can be inhibited.

[0076]

The foregoing description concerns the case in which all the signals at the position corresponding to the time stamp are set to 0 or 1 level. Alternatively, the same effect can be attained in the time stamp gate circuit 530 shown in Fig. 12 by changing at least a bit of the signal at the position of the time stamp. As a result, when the reproduced signal is recorded in another VTR, it is no longer possible to restore the packets to the original position. The dubbing can thus be inhibited.

[0077]

As header information other than the time stamp shown in Fig. 9(1), a control signal may be added in order for the receiver decoder to change the time stamp, the control signal being used for judging whether all bits of the output time stamp are changed to 0 or 1 level or whether at least one bit is changed.

[0078]

[Effects of the Invention]

According to the present invention, input digital information can be efficiently recorded, and a copy of reproduced signals can be inhibited easily.

[Brief Description of Drawings]

[Fig. 1]

Fig. 1 is a block diagram showing a digital broadcast system and an analog broadcast system to which the invention is applied.

[Fig. 2]

Fig. 2 is a block diagram showing a program distribution center according to an embodiment of the invention.

[Fig. 3]

Fig. 3 is a block diagram showing a program distribution center according to an embodiment of the invention.

[Fig. 4]

Fig. 4 is a block diagram showing a transmission processing device according to an embodiment of the invention.

[Fig. 5]

Fig. 5 is a block diagram showing a receiver decoder according to an embodiment of the invention.

[Fig. 6]

Fig. 6 is a block diagram showing a receiver decoder according to an embodiment of the invention.

[Fig. 7]

Fig. 7 is a block diagram showing a VTR according to an embodiment of the invention.

[Fig. 8]

Fig. 8 shows signal waveforms according to the invention.

[Fig. 9]

Fig. 9 shows signal waveforms according to the invention.

[Fig. 10]

Fig. 10 is a block diagram showing a time stamp adder circuit according to an embodiment of the invention.

[Fig. 11]

Fig. 11 shows signal waveforms according to the invention.

[Fig. 12]

Fig. 12 is a block diagram showing a temporal adjusting circuit according to an embodiment of the invention.

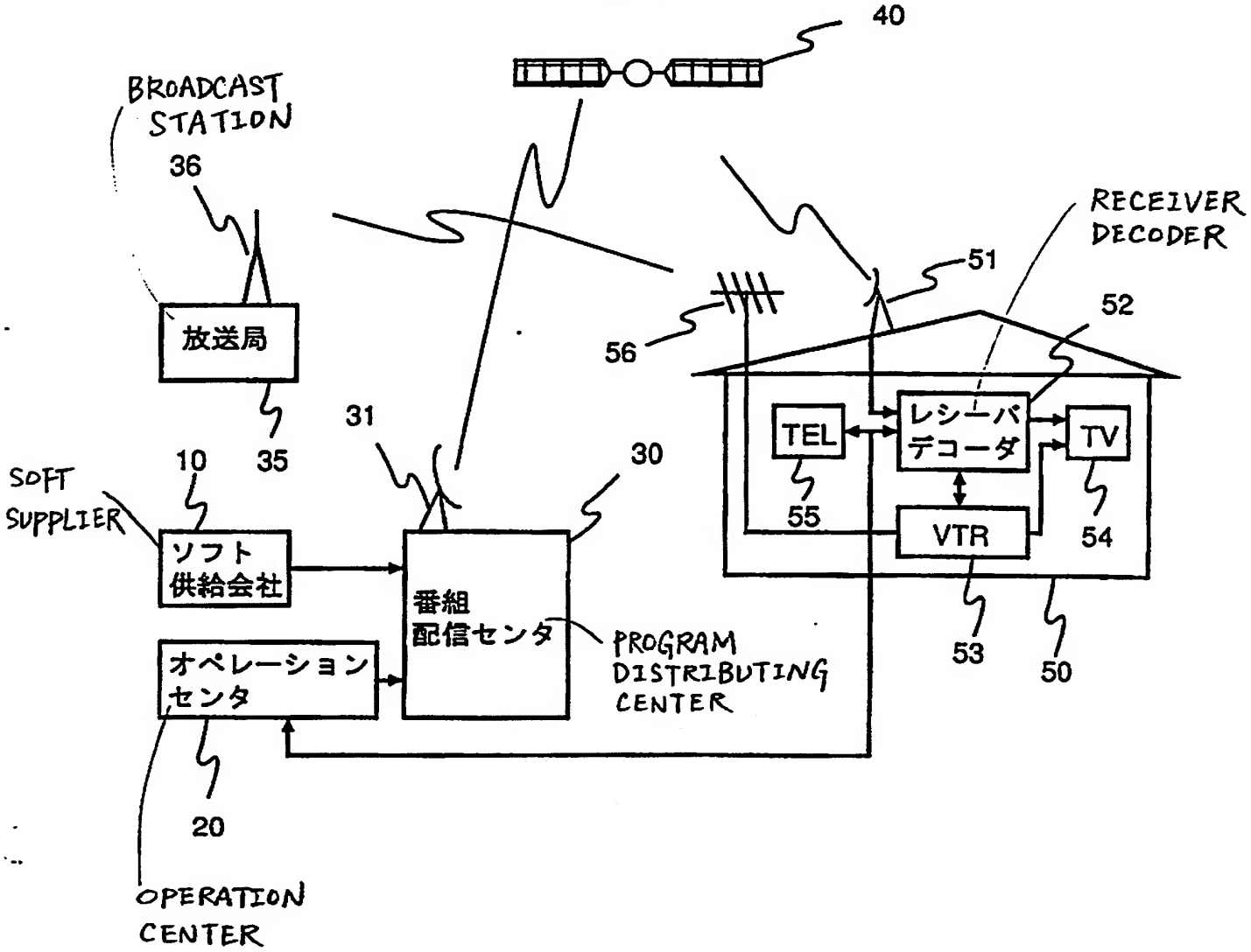
[Description of Reference Numerals]

52... receiver decoder, 53... VTR, 121, 130, 171 to 173... bit compressors, 140, 180... transmission processing device, 181 to 184... encryptor, 185... time-division multiplexer, 186... error correction code adder, 187... modulator, 220, 331... error correction circuit, 230... program dividing circuit, 250... dycryption circuit, 290, 305... interface circuit, 311... parity adder circuit, 530... time stamp gate.

〔TITLE OF DOCUMENT〕 DRAWINGS
【書類名】 図面

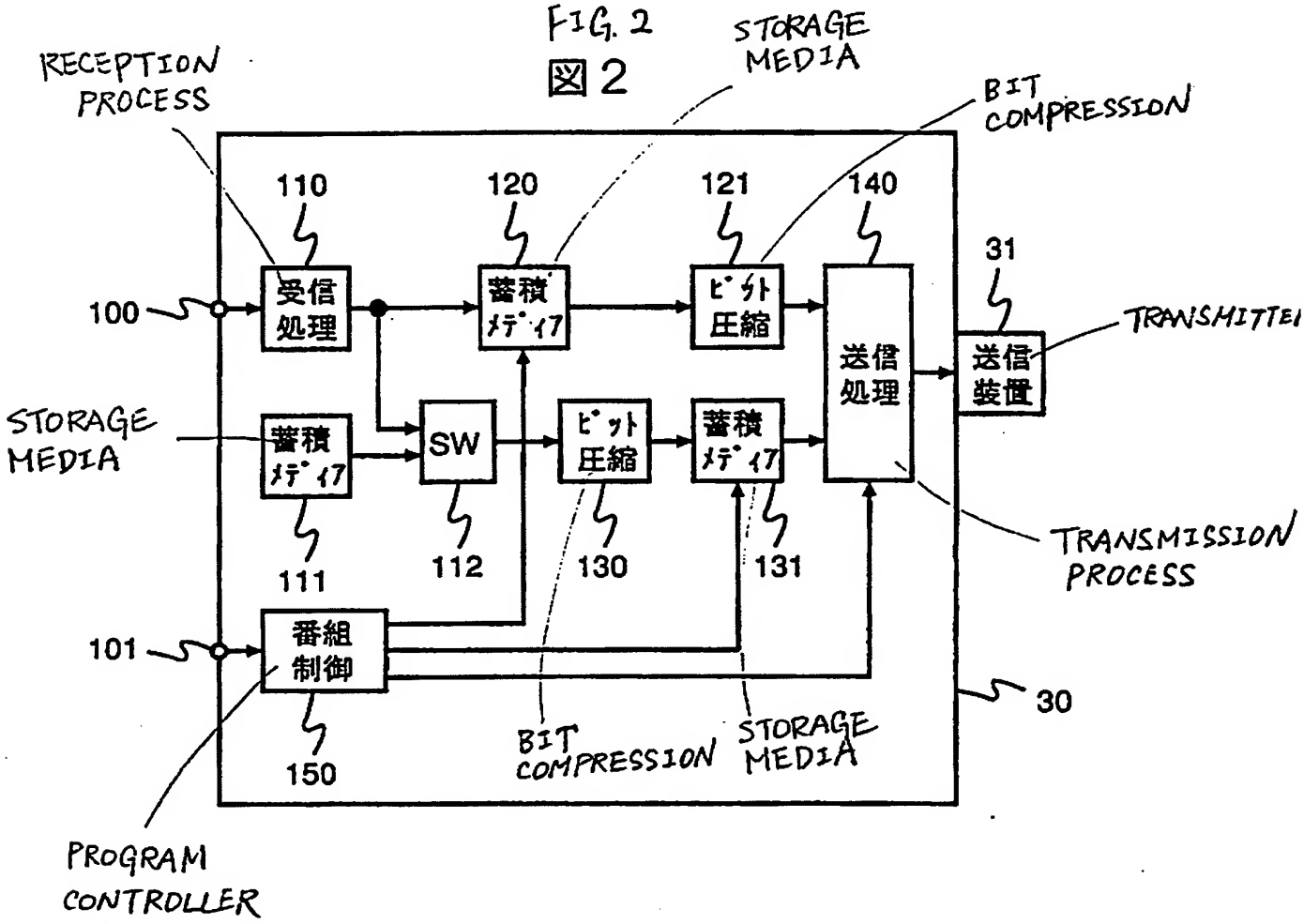
【図１】 〔FIG. 1〕

FIG. 1
図１



【図2】 〔FIG. 2〕

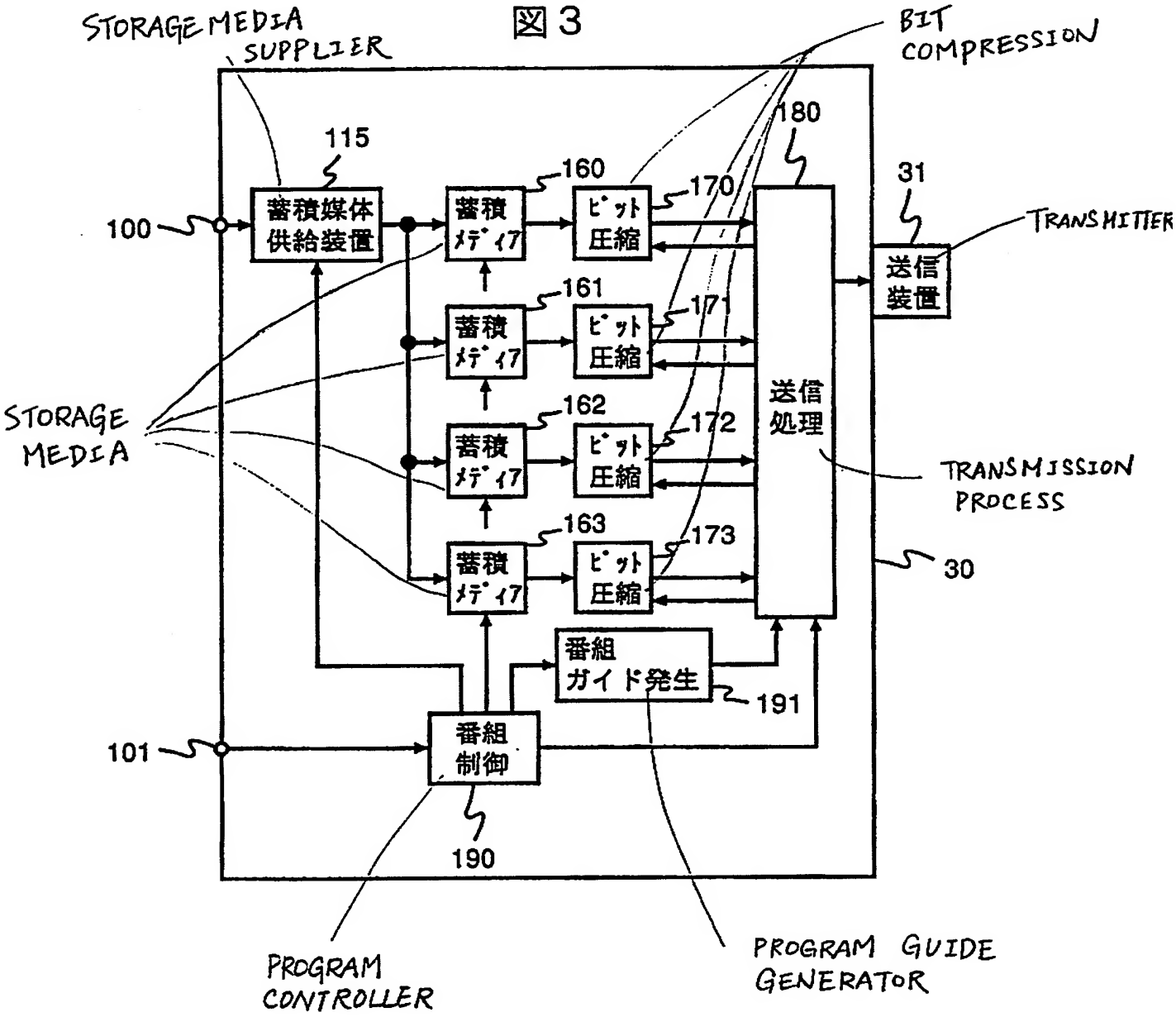
FIG. 2
図2



【図3】 [FIG.3]

FIG. 3

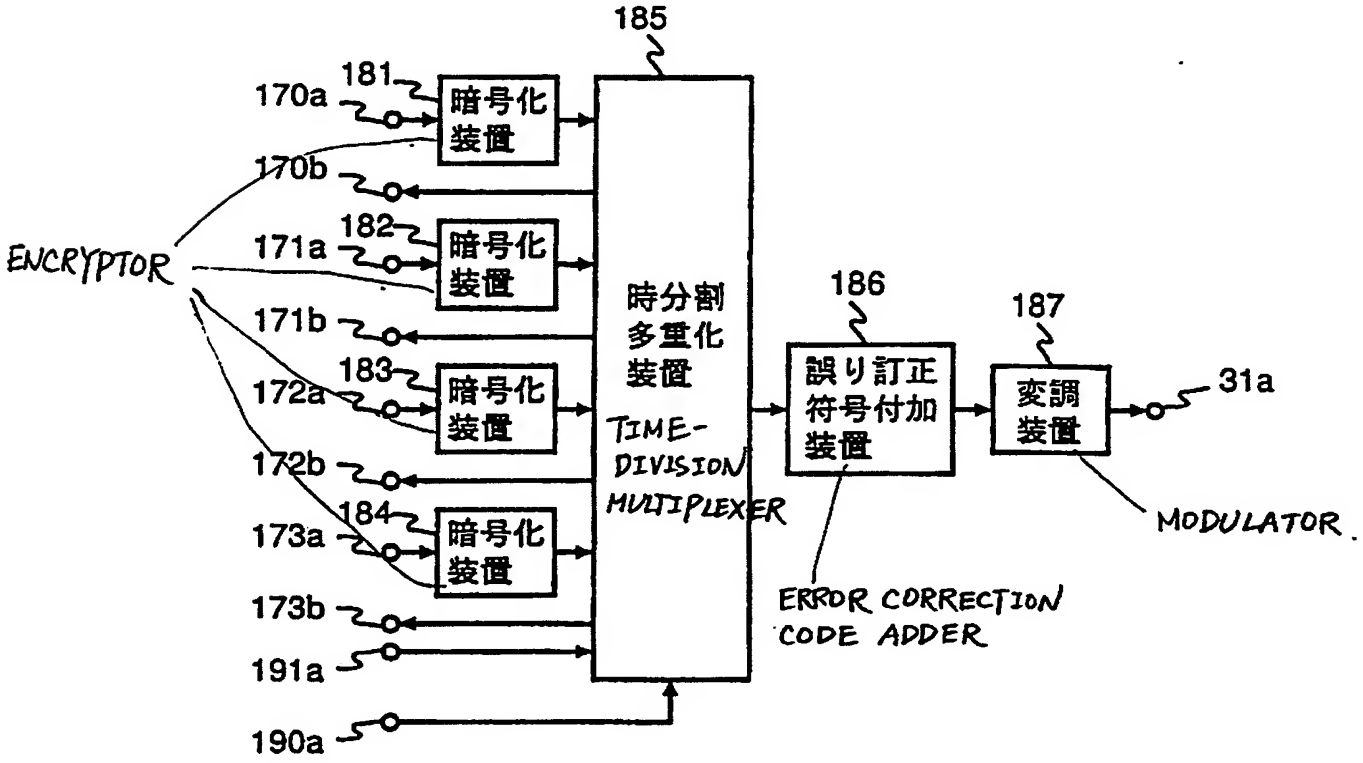
図3



【図4】 〔FIG.4〕

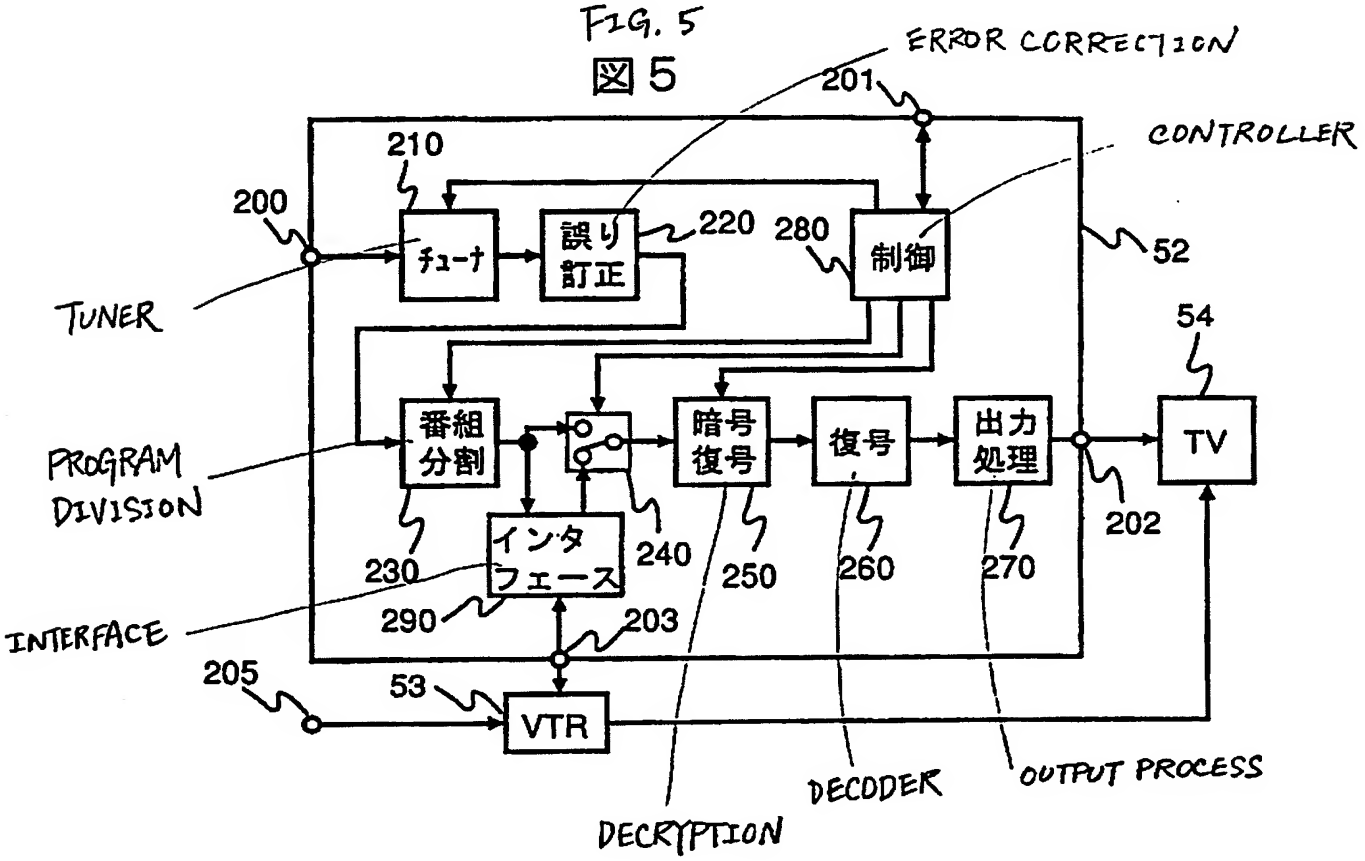
FIG.4

図4



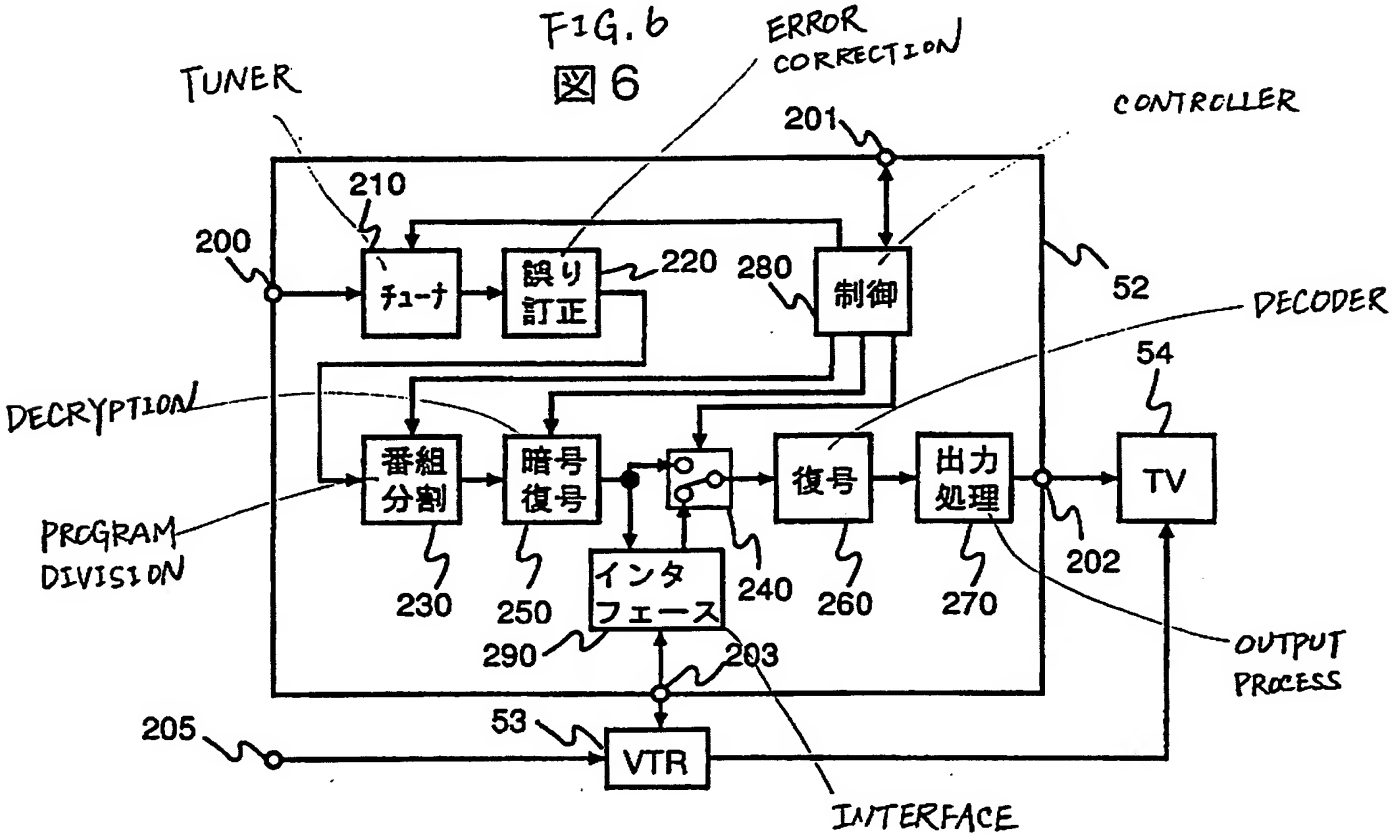
【図5】〔FIG. 5〕

FIG. 5
図5



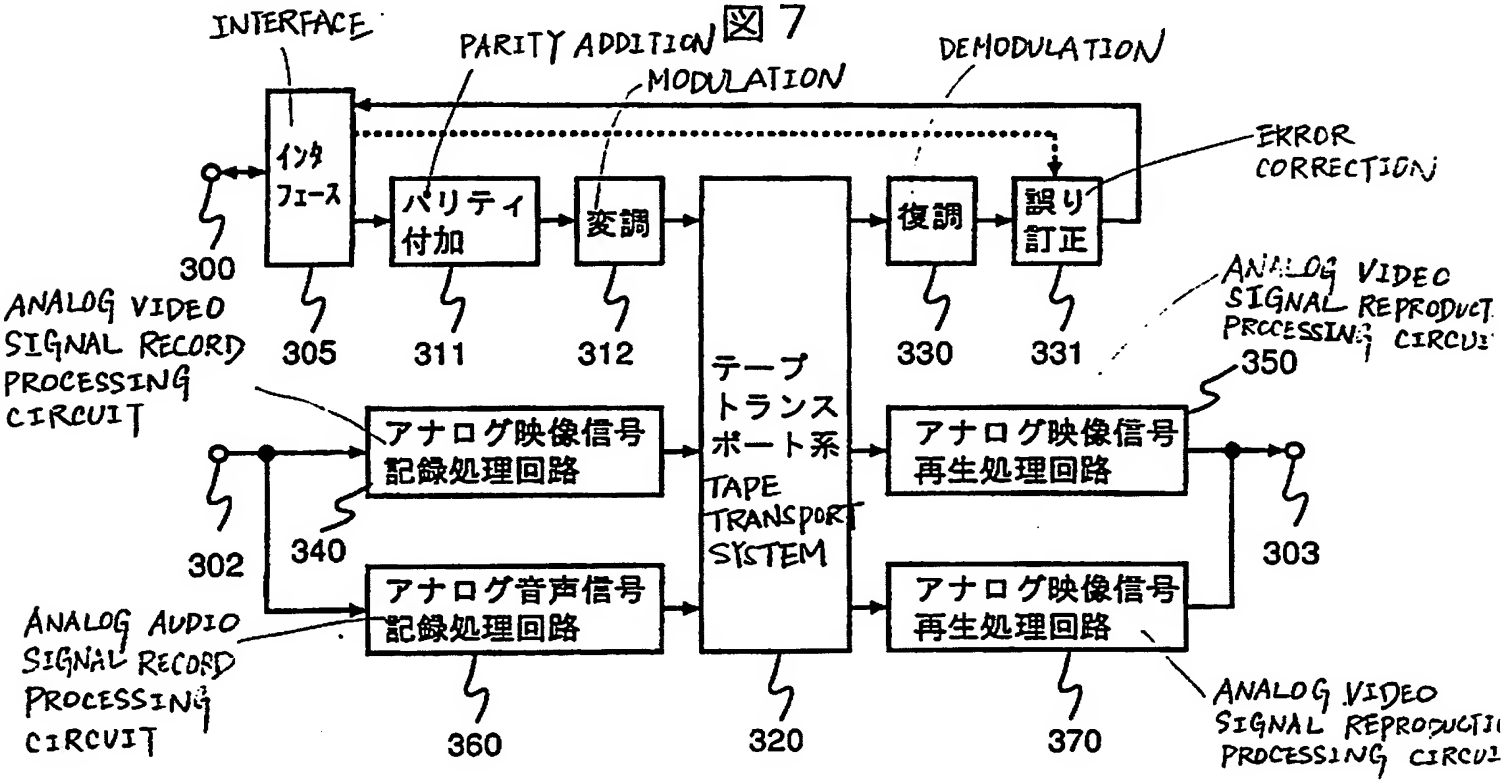
【図6】〔FIG.6〕

FIG.6
図6



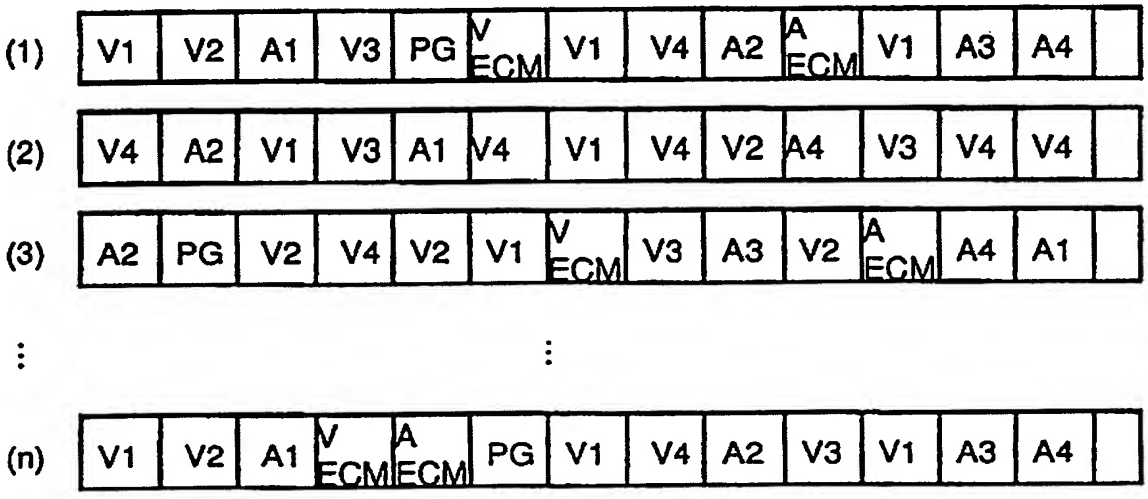
【図7】[FIG. 7]

FIG. 7
図7



【図8】[FIG. 8]

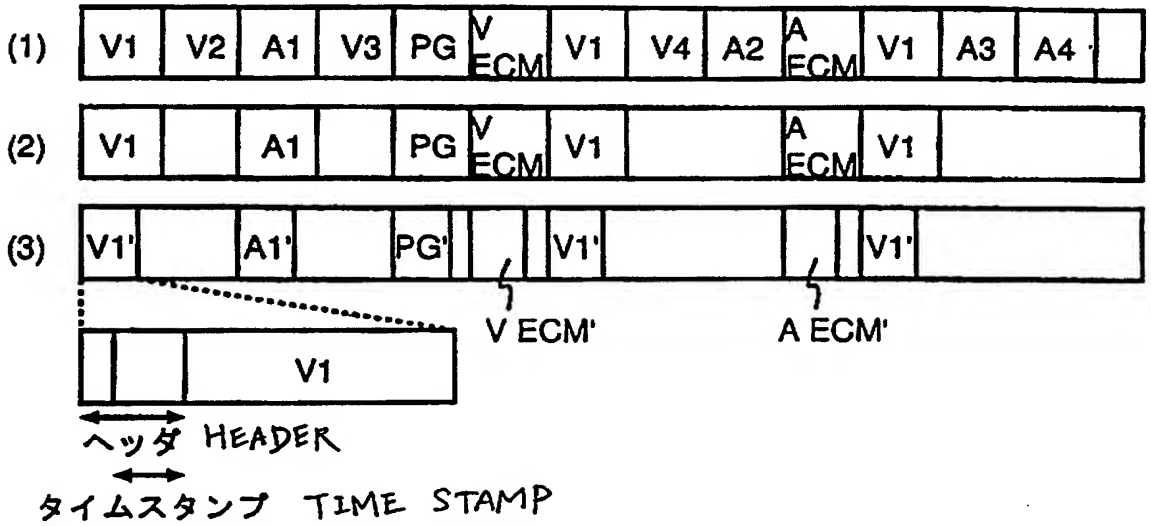
FIG. 8
図8



〔図9〕 〔FIG.9〕

FIG. 9

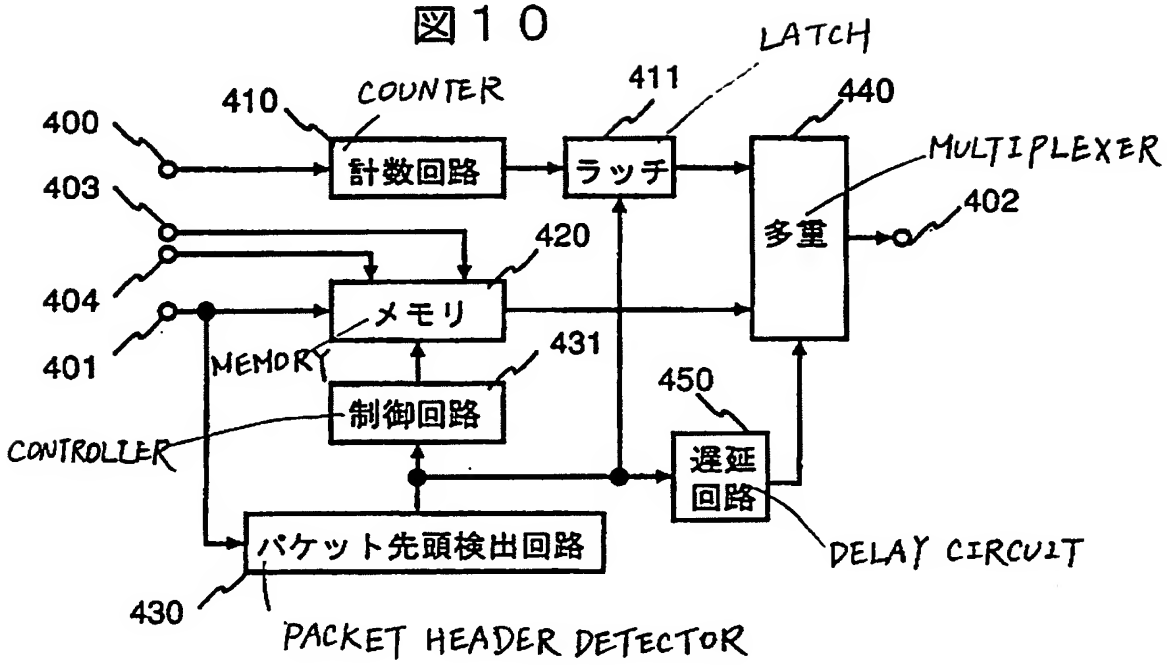
図9



〔図10〕 〔FIG.10〕

FIG. 10

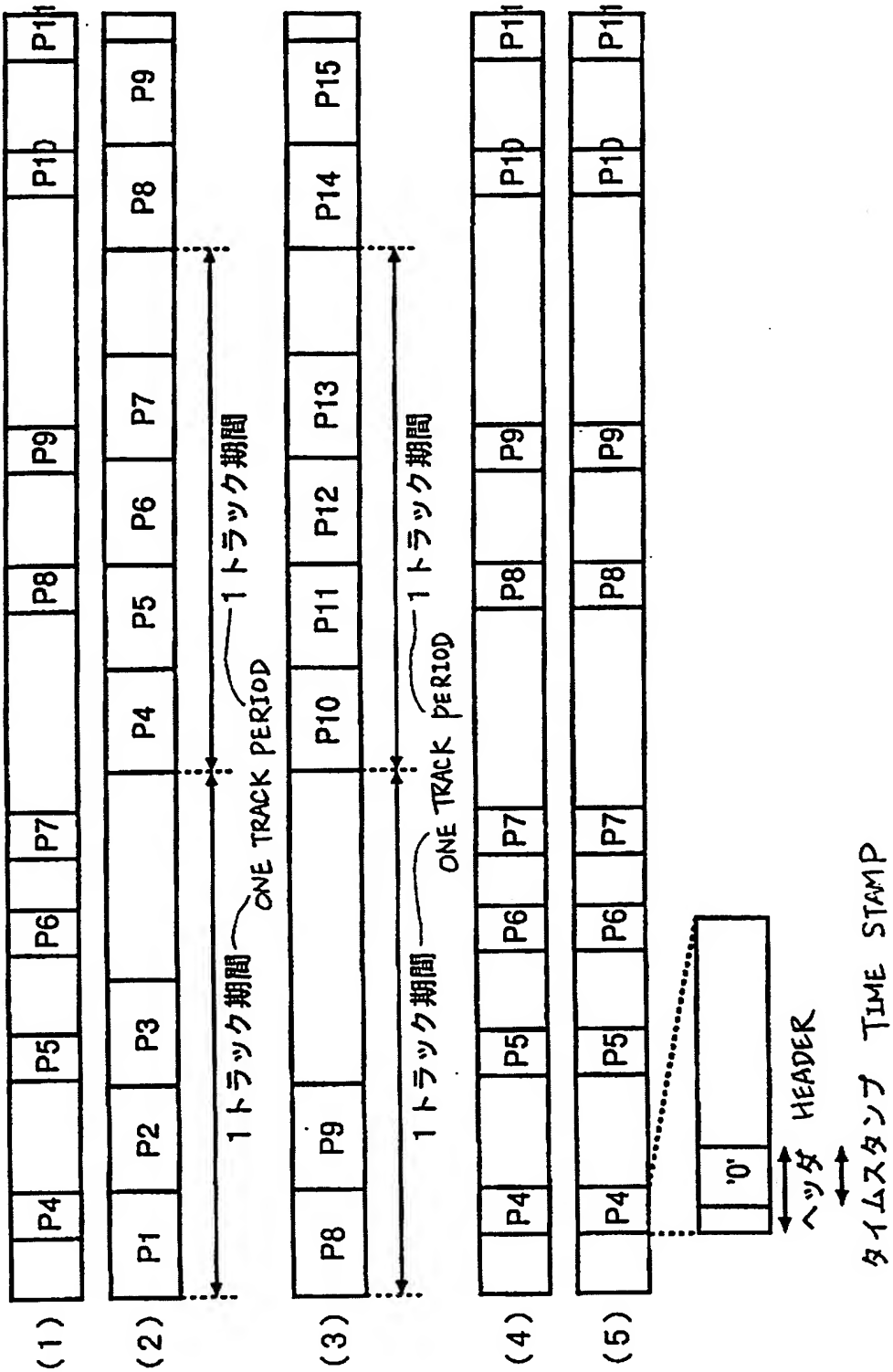
図10



【図１１】【FIG. 11】

FIG. 11

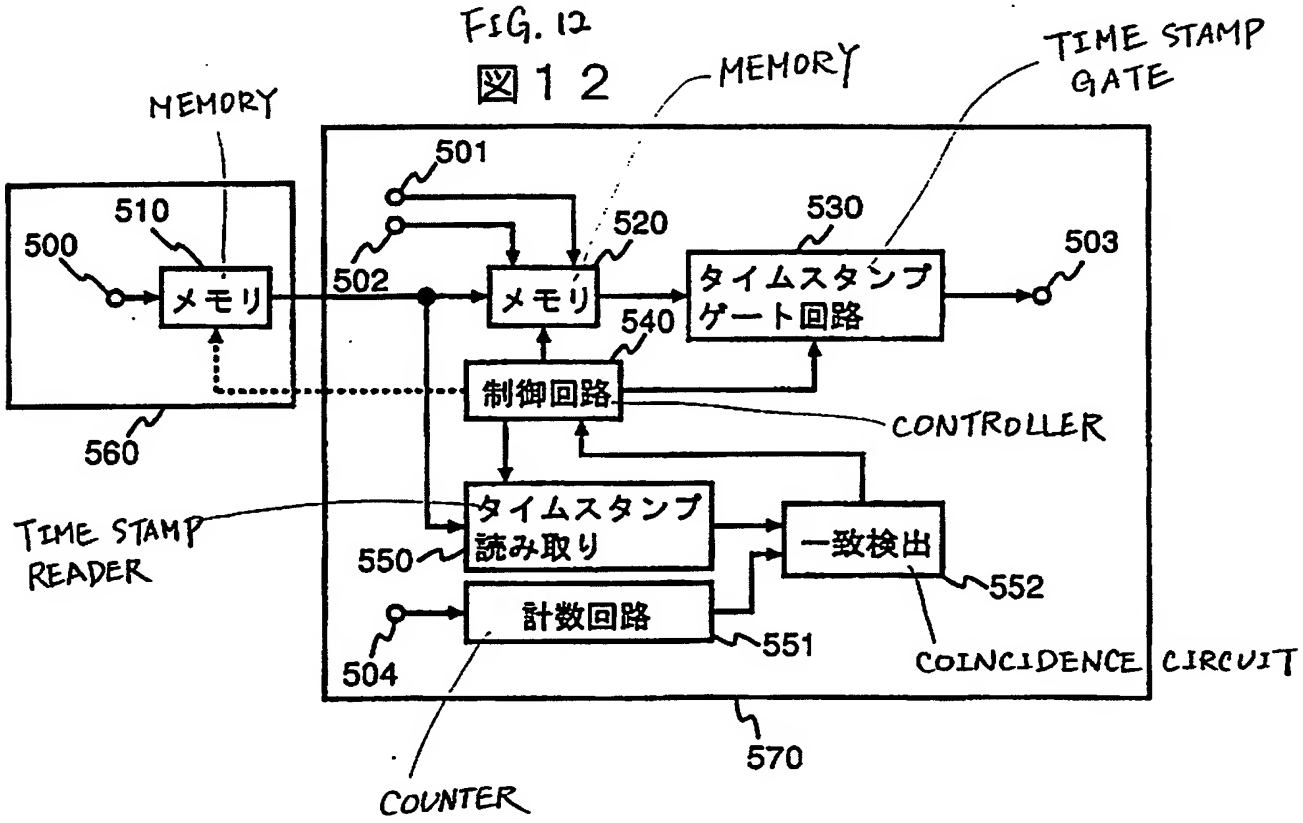
図１１



【図１２】　[FIG. 12]

FIG. 12

図１２



[Title of Document] Abstract

[Object]

Input digital signals in the form of packet can be efficiently recorded and a copy of recorded digital signals can be inhibited.

[Structure]

Time information is added to packet signals, and the packeted signals with time information are recorded at reduced intervals therebetween. In reproducing, the original packet intervals are recovered in accordance with the time information, and at least one bit of the time information is changed and thereafter output.

[Effect]

Since the packet intervals are reduced, the record efficiency can be improved. Even if the reproduced signals are recorded, normal signals cannot be output and a copy can be inhibited easily.

[Selected Drawing] Fig. 12

[Agent]

[Agent's ID Number] 1 0 0 0 6 8 5 0 4

[Postal Code] 100

[Address] c/o HITACHI, LTD., 5-1, Marunouchi-1-chome, Chiyoda-ku, Tokyo, Japan.

[Patent Attorney]

[Name] Katsuo OGAWA

[Telephone] 03-3212-1111

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